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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,453	11/01/2001	Hidetaka Magoshi	SCEISZ 3.0-105	3997

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,453	MAGOSHI, HIDETAKA	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 07/17/2006.

2. Claims 1-9 are pending in this application. Claims 1, 6, and 8-9 are independent claims. In Amendment, claims 10-13 are cancelled. This Office Action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakazawa (J.P. 07-141325).

Re claim 1, Nakazawa discloses in Figures 1 and 5-6 a parallel arithmetic apparatus (Figure 1 wherein each of FMACs {11 & 21}, {12 & 22}, {13 & 23}, {14 & 24} processes in parallel relative to each other) comprising:

a plurality of pair of devices (e.g. 11 with 21 as a pair of devices), each pair of devices including recording means (e.g. 11-14) for recording arithmetic elements (e.g. Aa and Ab from 10 to each of 11-14) to be operated and operating means (e.g. 21-24) for performing sum-of-products operations (e.g. 21 sum is done by 21B and product is done

by 21A) on the arithmetic elements recorded in the recording means (e.g. wherein operands of 21 are fed from 11); and

selecting means (e.g. multiplexers 30a, 30b, and 51a and 51b) having an input from each of the recording means and an output to only one of the operation means (e.g. only the multiplexers 30a , 30b, 51a, and 51b are considered as selecting means in Figure 1), the selecting means inputting arithmetic elements recorded in a selected one of the recording means (e.g. input to mux are from 11-14) to the one operating means (e.g. 21-24).

Re claim 2, Nakazawa further discloses in Figures 1 and 5-6 temporary recording means (e.g. a portion of 11-14 wherein the feedback from accumulators 21B-24B to 11-14 with label C) inserted between the recording means and the operating means in a second pair of devices different from the first pair of devices for temporarily recording mathematical elements recorded in the recording means of a pair of devices and selecting means (e.g. 30a and 30b) is constructed in such a way as to input the arithmetic elements recorded in temporary recording means to the one operating means (e.g. these mux are capable to input any of a or b from 11-14 into 21 as input operands).

Re claim 3, Nakazawa further discloses in Figures 1 and 5-6 the recording means of each pair of devices records, a first arithmetic element to be subjected to matrix operation, and a second arithmetic element to be subjected to inner product operation (Figure 1 is capable of performing matrix and vector operations, any input element would be either matrix element or the vector element), selecting means (e.g. 30a & 30b and 51ab-54ab) is adapted, during matrix operation (e.g. 51ab-54ab takes directly from 11-

14), to input first arithmetic element from the selected recording means to the one operating means and, during inner product operation (e.g. 52ab-54ab takes directly from 12-14 and 51ab takes inputs from 30a-30b), to select recording means of all pair of devicess one by one in a round-robin fashion and input second arithmetic element from the selected recording means to the one operating means (e.g. 12 to 22).

Re claim 4, Nakazawa further discloses in Figures 1-2 and 5-6 each of operating means in the pair of devices performs an operation with a content independently assigned to the pair of devices using arithmetic elements recorded in the recording means of pair of devices (e.g. each of registers 11-14 have their own pair of devicess of data as seen in Figure 2).

Re claim 5, Nakazawa further discloses in Figures 1 and 5-6 an operation is an operation associated with any one of four-dimensional coordinate components (Figure 6 with column as dimensions).

Re claim 6, Nakazawa discloses in Figures 1 and 5-6 a parallel arithmetic (Figure 1 wherein each of FMACs {11 & 21}, {12 & 22}, {13 & 23}, {14 & 24} processes in parallel relative to each other) apparatus that selectively performs a matrix operation (Figure 6a) and vector inner product operation (Figure 6b), comprising:

a plurality of recording means (11-14) for recording, during matrix operation, a first arithmetic element (e.g. output from 10 into 11 as Ab) to be subjected to matrix operation and recording, during inner product operation, a second arithmetic element (e.g. output form 10 into 11 as Aa) to be subjected to inner product operation;

a plurality of operating means (e.g. 21-24) forming a one-to-one correspondence with plurality of recording means (e.g. 11-14) for performing during matrix operation, a sum-of-products operation (e.g. 21-24) by each operating means inputting first mathematical element recorded in the correspondent recording means, and performing during inner product operation, a sum-of-products operation by predetermined one of the operating means inputting second arithmetic element recorded in all the recording means (e.g. using mux); and

selecting means (e.g. 30ab and 51ab-54ab) having an input from each of the recording means and an output to the predetermined operating means (e.g. only the multiplexers 30a , 30b, 51a, and 51b are considered as selecting means in Figure 1), the selecting means for selecting, during matrix operation (all mux 51ab-54ab are active), a first recording means corresponding to predetermined operating means and inputting a first arithmetic element recorded in the first recording means in predetermined operating means, and selecting, during inner product operation (e.g. mux 30ab active to 21), plurality of recording means one by one in a round-robin fashion (e.g. Figure 6) and inputting a second arithmetic element recorded in the selected recording means in predetermined operating means.

Re claim 8, it is an apparatus claim of claim 6 wherein Nakazawa further discloses in Figures 1 and 5-6 the recoding means, selecting means, and operating means are registers, selector, and sum of product respectively (e.g. 11, 30a, and 21 respectively). Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 9, it is an apparatus claim of claim 8 wherein Nakazawa further discloses in Figures 2 and 6 the arithmetic elements are the coordinate values (Figures 2 and 6). Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being obvious over Nakazawa (J.P. 07-141325).

Re claim 7, Nakazawa further discloses in Figures 1 and 5-6 the first and second arithmetic elements are expressed with a number and the plurality of operating means are constructed so as to perform a sum-of-products operation of the number (e.g. 21 with multiplication 21A and accumulation 21B). Nakazawa does not disclose the number is floating-point. However, the examiner takes an official notice that MAC operation in floating-point is well known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the number as floating-point as well known into Nakazawa's invention because it would enable to simplify and improve accuracy of system in many applications.

Response to Arguments

7. Applicant's arguments filed 07/17/2006 have been fully considered but they are not persuasive.

a. The applicant argues in pages 8-9 for all claims that the cited reference by Nakazawa fails to disclose the selecting means having an input from each of the recording means and an output to only one of the operating means as cited in the claim because the selecting means of the cited reference sends the output to all the operating means.

The examiner respectfully submits that generally the cited reference discloses narrower invention then the application's invention. Generally without extra the multiplexers 52-54 a and b, the cited reference's invention is the application's invention. Thus, invention in the cited reference contains or meets all the limitations cited in the claims 1-9 of the present invention. Basically, the selecting means is the only multiplexers 30a, 30b, 51a, and 51b in Figure 1 which output only one (e.g. as the output of the 51a and 51b to the selected operating means 21) of the operation means (e.g. 21-24 in Figure1).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

September 9, 2006

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
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